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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,611	02/12/2004	Andrew W. Martwick	42P6731C	4633

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EXAMINER	
PARK, ILWOO	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,611	MARTWICK, ANDREW W.	
	Examiner	Art Unit	
	Ilwoo Park	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-19 and 21-29* is/are rejected.

7)☒ Claim(s) *10,20 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on 12/12/2005, PROSECUTION IS HEREBY REOPENED. New Grounds of Rejections set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Terminal Disclaimer

2. The terminal disclaimer filed on 9/13/2005 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US patent No. 6,718,407 has been reviewed and is accepted. The terminal disclaimer has been recorded.

3. Claims 1-30 are presented for examination. Cooper et al., Estakhri et al., and Tanaka et al. were cited in the last office action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 11, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cooper et al., US patent No. 5,805,882 in view of Davis, US patent No. 5,844,986.

As to claims 1 and 11, Cooper et al teach a method and an apparatus comprising:

receiving [routine for the microcontroller 174 to receive and parse commands and data necessary to update the flash ROM 122 in col. 11, lines 19-37] a programming information to update [col. 3, lines 18-26] a firmware device [flash ROM 122], separated from a processor [CPU 100 in fig. 1], containing a boot code [BIOS in col. 5, lines 32-35; col. 9, lines 48-52] for the processor from a communication interface [parallel port 180]; and

parsing [col. 11, lines 19-37; fig. 10B] the programming information into control commands and program data by a parser.

Though Cooper et al, as seen in figs. 1 and 2, teach that the firmware device is only and directly connected to a chipset [mobile super I/O (MSIO) 120] and is only accessible through the chipset, Cooper et al do not teach the firmware device is in the chipset. Davis teaches a firmware device [non-volatile memory 42 in the form of field updatable BIOS flash memory in col. 1, lines 39-67 and fig.1] containing a boot code

[BIOS boo-up firmware] for a processor [host processor 30] within a chipset [cryptographic coprocessor in col. 3, lines 10-24] separated from the processor.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Cooper et al and Davis because they both teach a field updatable firmware device containing a boot code for a processor accessing the boot code through a chipset and the Davis' teaching of a firmware device included within a chipset would increase efficiency by reducing space rather than two separate chips of Cooper et al's portable computer.

3. As to claim 21, Cooper et al teach a system comprising:

a processor [CPU 100];

a firmware device [flash ROM 122]; and

a self-update firmware controller [MSIO 120] coupled to the firmware device to self update [col. 3, lines 18-26] the firmware device, the controller comprising:

a communication interface to receive [col. 11, lines 19-37] programming information to update the firmware device, separated from the processor, containing a boot code [col. 5, lines 32-35; col. 9, lines 48-52] for the processor, and

a parser coupled to the communication interface to parse [col. 11, lines 19-37; fig. 10B] the programming information into control commands and program data.

Though Cooper et al, as seen in figs. 1 and 2, teach that the firmware device is only and directly connected to a chipset [mobile super I/O (MSIO) 120] and is only accessible through the chipset, Cooper et al do not teach the firmware device is in the chipset. Davis teaches a firmware device [non-volatile memory 42 in the form of field

updatable BIOS flash memory in col. 1, lines 39-67 and fig.1] containing a boot code [BIOS boo-up firmware] for a processor [host processor 30] within a chipset [cryptographic coprocessor in col. 3, lines 10-24] separated from the processor.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Cooper et al and Davis because they both teach a field updatable firmware device containing a boot code for a processor accessing the boot code through a chipset and the Davis' teaching of a firmware device included within a chipset would increase efficiency by reducing space rather than two separate chips of Cooper et al's portable computer.

4. Claims 2-9, 12-19, and 22-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cooper et el and Davis as applied to claims 1, 11, and 21 above, and further in view of Tanaka et al., US patent No. 6,266,810.

As to claims 2, 12, and 22, Cooper et al and Davis teach programming the firmware device based on the control commands by control logic circuit [mobile super I/O 120 of Cooper et al]. However, Cooper et al and Davis do not explicitly disclose a buffer to store the program data to be written into the firmware device.

Tanaka et al teach a buffer [col. 4, lines 40-45] to store a program data to be written into a firmware device [flash ROM 101].

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the Tanaka et al's teaching of the buffer to store the program data to be written into the firmware device in order to increase flexibility in timing for programming the firmware device of Cooper et al and Davis.

5. As to claims 3, 13, and 23, Cooper et al teach providing the programming information to the parser by a source selector [fig. 2; col. 7, lines 38-54].

6. As to claims 4, 14, and 24, Cooper et al teach selecting one of the programming information [col. 7, lines 38-54] from the communication interface and an input and output (I/O) channel data [col. 7, lines 41-44] by a multiplexor [multiplexor 178].

7. As to claims 5, 15, and 25, Cooper et al teach erasing [col. 13, lines 51-54] the firmware device by an erase control circuit and Tanaka teaches writing [col. 4, lines 35-39] to the firmware device using the program data in the buffer by a write control circuit.

8. As to claims 6, 16, and 26, Cooper et al teach generating the control commands based on the parsed programming information by a state machine [col. 11, lines 19-37; fig. 10B], the control commands including [col. 13, lines 46-54] at least an erase command and a write command.

9. As to claims 7, 17, and 27, Cooper et al teach the programming information includes at least a self-update identifier [col. 12, line 61-col. 13, line 3], program parameters [col. 14, lines 6-8], and program data [col. 14, lines 15-16].

10. As to claims 8, 18, and 28, Cooper et al teach recognizing [col. 12, line 61-col. 13, line 3] the self-update identifier, reading [col. 14, lines 6-8] the program parameters including at least erase, and write addresses and generating an erase command to the erase control circuit to a block [col. 13, lines 20-32] in the firmware device at the erase address, and Tanaka et al teach generating a buffer write command to write [col. 4, lines 40-45] the program data into the buffer and generating a write command to the

write control circuit to the program data in the buffer to the firmware device at the write address [col. 4, lines 35-39].

11. As to claims 9, 19, and 29, Cooper et al and Davis do not disclose converting serial data [packet] into the programming information by a serial to parallel converter; in fact, Cooper et al and Davis teach receiving the programming information in parallel form through the parallel communication interface. Tanaka et al implicitly teach converting serial data [packet stream] into the programming information by a serial to parallel converter. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include Tanaka et al's teaching of receiving and converting serial data into the programming information by a serial to parallel converter in order to increase flexibility by adapting prevalent serial interface.

Allowable Subject Matter

12. Claims 10, 20, and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ilwoo Park whose telephone number is (571) 272-4155. The examiner can normally be reached on Monday through Friday from 9:00 AM to 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ILWOO PARK
PRIMARY EXAMINER

Ilwoo Park
February 17, 2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER